Multiplexing cross-connector E1-DXC

Features

- Desktop or the card for 19" 3U Cronyx rack
- Four E1 links (PCM-30)
- Distance up to 1,5 km (up to 2,5 km for rack design)
- 128 x 128 non-blocking switching matrix
- G.704 frame structure
- CAS and CRC4 multi-frame structure
- Sa bits cross-interchange
- Clock source from the built-in oscillator, from any E1 receiver, or from the digital interface
- Master and backup clock
- Synchronous V.35, RS-530, RS-449, RS-232, X.21, Ethernet interface, or and IDSL modem in place of one of the E1 links
- Asynchronous mode for the RS-232 interface
- Built-in HDLC buffer for models with a synchronous V.35, RS-530, RS-449, RS-232, or X.21 interface
- Local loop
- Digital loop for models with a V.35, RS-530, RS-449, RS-232, or X.21 interface
- Built-in Bit Error Rate Tester (BER tester);
- RS-232 port for monitoring and control
- "Dry contact" alarm signaling (for desktop models only)
- Built-in power supply unit from mains or battery
- Upgradable firmware
- SSE Certificate of the State Communications Committee of the Russian Federation No. OS/1-SPD-19

Contents

Technical specifications

Digital interface

Data transmission rate ..... 64 to 1984 kbit/sec (Nx64)
Clock signals ..... TXC, RXC, ETC, ERC
Modem signals ..... DTR, DSR, CTS, RTS, CD

Ethernet interface (for the E1-DXC/B/3E1-ETH model)

Interface type, connector ..... 10BaseT, RJ-45 (female)
Bandwidth ..... 64 to 1984 kbit/sec (Nx64)
Operating modes ..... Half Duplex or Full Duplex
Filtering rate ..... 15000 frames per second
Maximum frame size ..... 1518 bytes, including the MAC layer header and the CRC
LAN table size ..... 10000 MAC-addresses

Ethernet interface (for the E1-DXC/B/3E1-ETV model)

Interface type, connector ..... 10/100BaseT, RJ-45 (female)
Bandwidth ..... 64 to 1984 kbit/sec (Nx64)
Operating modes ..... 100 Mbps Full Duplex, 100 Mbps Half Duplex, 10 Mbps Full Duplex, 10 Mbps Half Duplex, or Autonegotiation
LAN table size ..... 15000 MAC-addresses
Maximum frame size ..... 4228 bytes, including the MAC layer header and the CRC
Protocols ..... Transparent or Cisco-HDLC bridging IEEE protocol, automatically selected

E1 interface

Encoding HDB3
Line impedance
- 19" rack design ..... 120 Ohms, symmetrical (twisted pairs)
- for desktop design ..... 120 Ohms symmetrical (twisted pairs), or 75 Ohms unsymmetrical (coaxial), jumper-selectable

Signal level at the receiver input
- for desktop design ..... 0 to -36 dB (up to 1,5 km over 0,6 mm twisted pairs)
- for rack design ..... 0 to -43 dB (up to 2,5 km over 0,6 mm twisted pairs)

Transmitter path synchronization ..... from the built-in oscillator, or from the E1 link receiver, or from the digital port
Jitter attenuator ..... in the receiver or transmitter path, attenuation up to 120UIpp
Frame,.multi-frame structure ..... according to G.704 (CRC4, CAS multi-frames)
Link rate negotiation ..... elastic store slip buffers in receiver paths
Connector ..... removable terminal

Emergency alarm interface (for desktop design models)

Relay contact current ..... up to 250 mA
Relay contact voltage ..... up to 175 VDC
Connector ..... Mini DIN, 6 pins (female)

Control port

Interface type, connector ..... RS-232, DB9 (female)
Data transmission protocol ..... asynchronous, 9600 bit/sec, 8N1

Diagnostic modes

Loops ..... local (on the G.703 line) or digital (on the digital interface) enabled via the control port
BER-tester ..... enabled via the control port

Description

The Cronyx E1-DXC multiplexing cross-connector is designed for timeslot interchange between any of the four E1/PCM30 links. Interchange is performed according to a user-specified map.

According to the selection made by the user, one of the E1 ports of the multiplexing cross-connector may be replaced by a RS-530, RS-232, V.35, or X.21 interface with standard connectors, by a universal interface, or by a built-in Ethernet module or IDSL modem. The universal interface supports RS-232, RS-530, RS-449, RS-422, V.35, and X.21 standards, and is equipped with a HDB44 connector (MDS36 connector in 19" rack design models), the interface type in this case is determined by the connected cable. Cronyx E1-DXC with Ethernet interface contains the Remote Bridge module, and may be used together with another Cronyx E1 series device equipped with Ethernet interface for interconnection of two LANs.

In order to provide proper data transmission, the multiplexing cross-connector provides equal delay for timeslots constituting the common data transmission link.

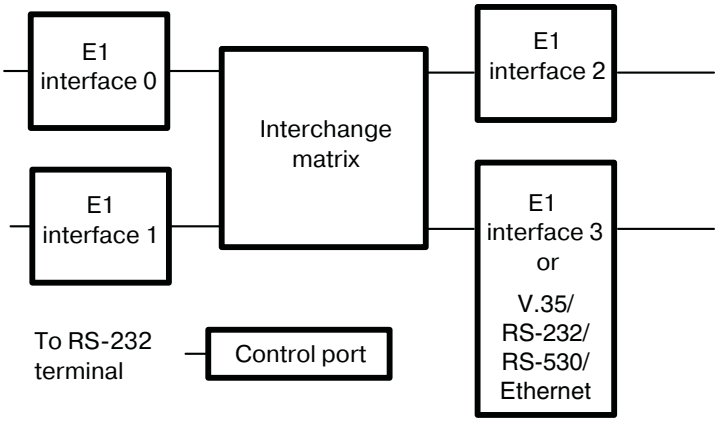
The multiplexing cross-connector configuration settings are performed via the control port equipped with RS-232 interface (control and monitoring for rack design models is possible via RMC board). Configuration parameters are stored in EEPROM of the device.

Capability to enable loops over E1 links is provided for testing E1 links.

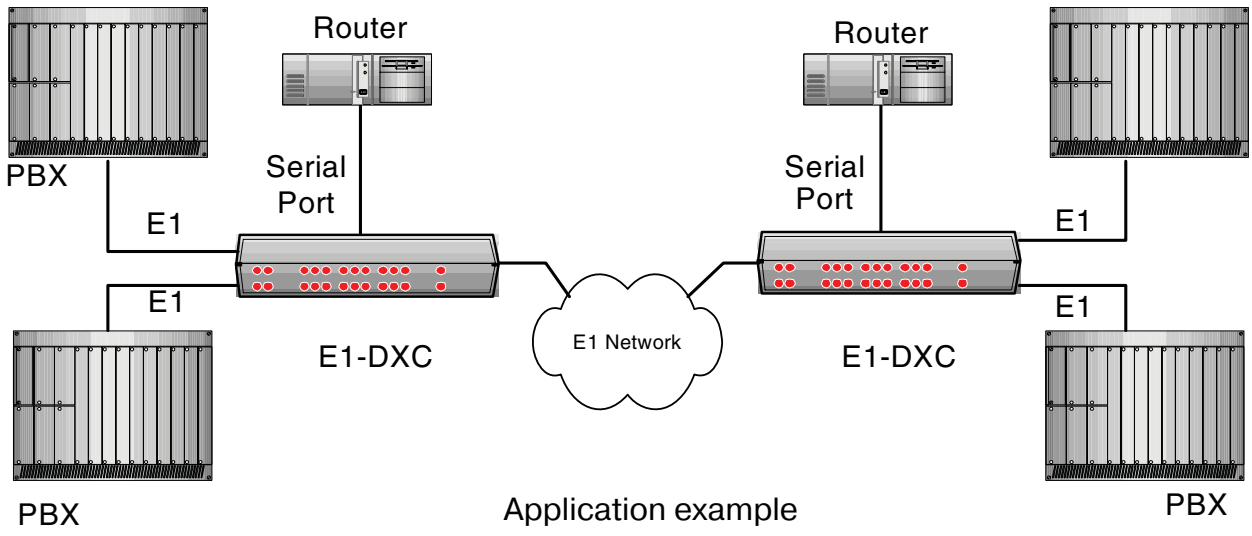
The multiplexing cross-connector has the capability to upgrade its firmware via the console port. New firmware revisions allow to expand multiplexer's capabilities. Loading special firmware revisions allows to change multiplexer's functional capabilities completely. Upgrades are available from the Cronyx Web-server - www.cronyx.ru.

Device structural diagram is presented below.

Below is an example of using E1-DXC. The figure shows the simultaneous connection of routers and office exchanges over a single link.



Device diagram



Application example

Delivered items

Delivered items include:

- The E1-DXC multiplexing cross-connector
- Removable terminals for connecting to E1 lines — 4 pcs. (3 pcs. for models equipped with a digital port)
- Power cable (for desktop design models with AC mains power supply)
- User's guide

Firmware upgrade

The multiplexer's firmware may be upgraded using a PC and special software, via console port. The firmware is available from Web-server located at www.cronyx.ru. The detailed loading procedure instructions are supplied with the firmware.

Order code

Design:
B - desktop
R - for 19" rack

E1-DXC/B/3E1-V35-AC

Model:

E1-DXC/B/4E1, E1-DXC/R/4E1 - four E1 ports

E1-DXC/B/3E1, E1-DXC/R/3E1 - three E1 ports and one digital interface

Power supply
(desktop design)
AC - ~220V
DC - =22...75V

Digital interface
(for /3E1 model)
530 - RS-530
232 - RS-232
V35 - V.35
X21 - X.21
M - universal
IDSL - ISDL modem
ETH - ethernet 10Base-T
ETV - ethernet 10/100Base-T

Controls and indicators

Front panel indicators

The PWR indicator shows the mains power supply.

The DI indicator (for rack design models only) shows the presence of the interface board.

Two indicators are used to show the status of each of the four ports: LINK (green) and ERR (red).

The LINK lights when the line carrier is present (for an E1 port), if the cable is connected (for the Ethernet port), or shows the RTS signal status (for the digital port). When loop or BER tester is enabled, the corresponding LINK indicator flashes.

The ERR indicator of the E1 port lights during line signal loss, during frame of multi-frame synchronization loss, or when there are errors in the line, if the BER tester is enabled. The ERR indicator flashes if there is a loss of frame (bit A of timeslot zero) or CAS multi-frame (bit of timeslot 16) synchronization on the remote device.

The ERR indicator of the Ethernet port lights during the overflow of bridge internal buffers.

The ERR indicator of the serial port lights during FIFO buffers overflow or underflow.

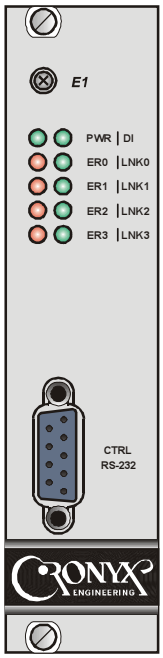
During loss of the master clock, the device switches to the backup clock source, and the LINK and ERR indicators of the corresponding port flash. If both clocks (master and backup) are lost, the device switches to the internal oscillator, then the LINK and ERR indicators of the source ports will flash.

Jumpers

Jumper location on multiplexer's printed circuit board is shown on figures below.

In order to move jumpers in desktop design devices, the device upper cover should be taken off after removing mounting screws.

Attention!!! Before removing the cover, make sure the device is disconnected from the power source.



Front panel of the 19" rack design device

Front panel of the desktop design multiplexing cross-connector

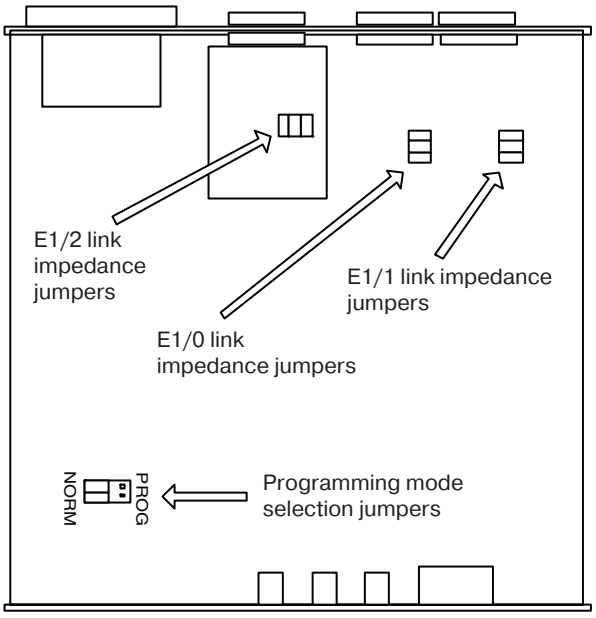
Line impedance

The desktop design multiplexer is delivered in configuration for twisted pair (120 Ohms) . E1 line impedance is selected by jumpers, there are three jumpers per link. The jumpers must be removed for twisted pair, and installed for coaxial cable (75 Ohms).

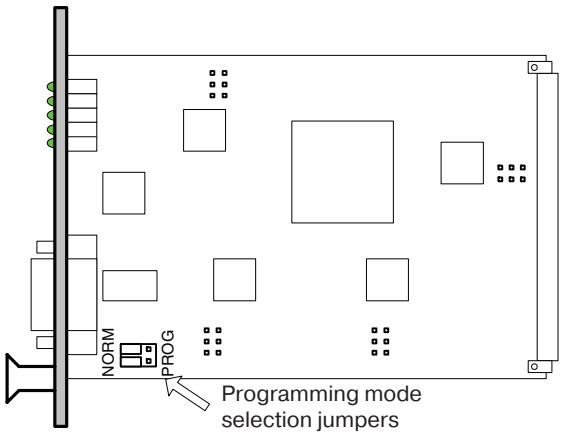
The 19" rack design multiplexing cross-connector is not equipped with line impedance selection jumpers, and is designed to operate over twisted pairs (120 Ohms)

Programming mode

Before loading a new firmware revision, two internal jumpers must be switched from the "NORM" position to the "PROG" position. After completing the programming procedure, the jumpers must be returned to the "NORM" position.

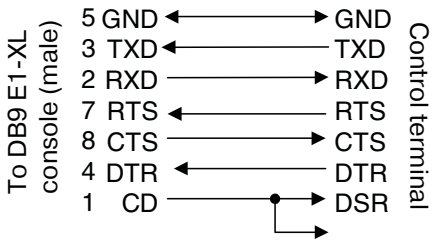


Jumper locations for desktop design models

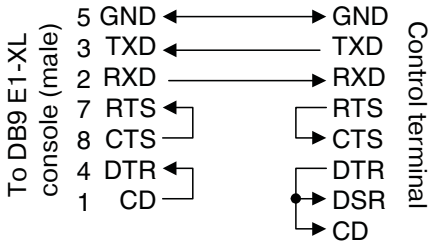


Jumper locations for 19" rack design models

The console connector has a standard pinout. When connecting the terminal, the presence of CD and CTS signals must be provided. It is recommended to use the following cable diagrams:



Cable with modem control



Cable w/o modem control

Console

The front panel of the multiplexer is equipped with a DB9 connector for connecting a control terminal (console) with a RS-232, 9600 bit/sec, 8 bits, no parity interface. The console may be used for viewing current device modes, link states, error statistics, for selecting device modes, and for storing them in the nonvolatile RAM.

Configuration parameters

Each time the multiplexing cross-connector is switched on, it is configured according to specified parameters. The configuration parameters specified from the console, are stored in the NVRAM.

Saving settings

Device parameters are stored in the nonvolatile RAM (NVRAM). When the device is switched in, the last saved parameters are set.

Device synchronization

The synchronization source may be one of the following:
- internal oscillator (Int)
- any of the E1 links (Link...)
- digital port (Port, for equipped models).

The master clock and the backup clock are specified for the device. When the master clock is lost, the device switches to the backup one. If both master and backup clocks are lost, the device switches to the internal oscillator.

Attention! The digital port should not serve as the backup clock.

Timeslot 16 mode

The sixteenth timeslot may be used for data transmission (Data) or for telephone signaling transmission (CAS).

Timeslot interchange map

When editing the Timeslot Interchange Map there is a capability to direct data from any incoming timeslot to any outgoing one. The delay mode is specified during this:

- Voice (minimum delay mode). This mode is used for timeslots containing independent 64 kbit/sec data streams (such as voice data).
- Data (fixed delay mode). This mode must be selected for all timeslots, which are used to transmit a common N x 64 kbit/sec data stream (N > 1). Otherwise, the integrity of this data stream may be violated.

Attention! The fixed delay mode is always selected in rack design models.

Sa bits interchange map

The Sa bit interchange map (S_{a4}-S_{a8}) may be specified in the multiplexing cross-connector. The Sa bit source may be any Sa bit of any E1 link, or the value of "1" is transmitted in the corresponding position.

Receiver path sensitivity

E1 link receiver path sensitivity may be set to one of the following two values: -12 or -36 dB (-43 dB for rack design models).

CRC4 multi-frame synchronism

When specifying configuration parameters for each E1 port, it is possible to enable or disable CRC4 multi-frame synchronization control.

Idle Code

When specifying the interchange map, the idle code is specified in non-interchanged timeslots. The idle code is entered and displayed in hexadecimal format, and is specified for each E1 port.

Loss of synchronization action

When specifying configuration parameters, it is possible to select on of the two responses to loss of E1 link synchronization:

- Remote Alarm - bit A of timeslot zero is set in the transmitted E1 frame.
- AIS - the AIS alarm indication signal ("blue code") is transmitted.

Digital port asynchronous mode

The digital port may support both the asynchronous and the synchronous data transmission modes. When specifying port configuration parameters in the asynchronous mode, one of the following rates may be selected: 1200, 2400, 4800, 9600, 19200, 38400, 57600, or 115200 bit/sec. The 8N1, 7P1, 8P1 asynchronous symbol formats are supported.

HDLC buffer

For information that is more detailed see section **"Synchronous data transmission"**.
This parameter is not used for Ethernet interface multiplexer.

Clock inversion

In models equipped with the digital port, when using INT or From Link clock, the TXD data are delayed in relation to the TXC clock. The total time shift is comprised of the delay in the cable, and the delay in the digital interface of the equipment connected to the E1-DXC. As a result, data errors may appear when selecting some rates.

This problem may be solved in the following way:

- TXC inversion by changing settings of the equipment connected to the E1-DXC;
- change of cable length;
- reversal of TXC-a and TXC-b pins on one of the interface cable connectors;
- selecting TxC clock inversion.

The same problem may appear when using external clock from the ERC receiver path. It may be solved in the same way:

- change of cable length;
- reversal of ERC-a and ERC-b pins on one of the interface cable connectors;
- selecting ERC clock inversion.

For information that is more detailed see section **"Synchronous data transmission"**.

Receiver path synchronization

Receiver path synchronization for the digital port may be set to one of the following modes:

- from E1 link receiver
- from external clock (ERC)

The receiver path synchronization from the external source mode is used when connecting to DCE devices, which do not have external synchronization from the digital port (RS-232, V.35, RS-530) mode. In this case the modem outputs clock data received at the ERC input. The FIFO buffer is used to correct data phase at the RXD digital port output in relation to ERC clock. For the correct operation of the buffer (no overflows or underflows), the clock frequency received from the line must be the same as the frequency at the ERC input. This condition is maintained when the data transmission link has a common clock source. Otherwise there may be periodic errors related to FIFO buffer overflows or underflows. The frequency of these errors depends on the discrepancy value between these two frequencies. In cases when it is not possible to provide common clock, and the data transmitted over the network comply with the HDLC protocol, the HDLC mode of the FIFO buffer must be used.

CTS generation logic

When specifying configuration, it is possible to select one of the four rules for CTS output signal generation:

CTS=1, CTS=CD, CTS=RTS, or CTS=CD*RTS.

Ethernet packet filtering

In some cases Ethernet packet filtering must be disabled for network administration, monitoring or testing purposes.

When filtering is enabled, the Ethernet bridge is used only to transmit frames filtered by destination addresses. When filtering is disables, all frames are translated from one side of the bridge to the other.

Ethernet interface mode

The Ethernet interface in the E1-DXC/B/3E1-ETH model operates at a fixed rate (10 Mbps), and there is the capability to select Half Duplex or Full Duplex mode.

In the E1-DXC/B/3E1-ETV model there is the capability to select data transmission rate (10 Mbps or 100 Mbps), Half Duplex or Full Duplex mode, or select autonegotiation mode.

DTE emulation

Two clock inputs - reception and transmission (ETC and ERC) are provided for connecting the E1-DXC multiplexer over RS-232, V.35, RS-530 interfaces to DCE devices in the synchronous mode. Only ETC is provided for the X.21 interface.

DTE1 emulation mode

The DTE1 emulation mode is used when connecting to DCE devices, which have external synchronization from the digital port (RS-232, V.35, RS-530, X.21) mode. In this case, a pair of devices connected over the digital port (RS-232, V.35, RS-530, X.21) transparently translates the clock frequency.

DTE2 emulation mode

The DTE2 emulation mode is used when connecting to DCE devices, which do not have external synchronization from the digital port (RS-232, V.35, RS-530) mode. In this case the E1-DXC multiplexing cross-connector receives data to the digital port according to the clock received on the ETC input, and transmits according to the clock received on the ERC input. The FIFO buffer is used to correct data phase at the RXD digital port output in relation to ERC clock.

For the correct operation of the buffer (no overflows or underflows) the clock frequency received from the line must be the same as the frequency at the ERC input. This condition is maintained when the data transmission link has a common clock source. Otherwise there may be periodic errors related to FIFO buffer overflows or

Configuration parameters

General parameters

Master clock ..... INT, Link0, Link1,Link2, Link3 (Port)
Backup clock ..... INT, Link0, Link1,Link2, Link3
Timeslot 16 ..... CAS, Data
Timeslot interchange map ..... non-blockable 128 x 128 interchange matrix
Sa bits interchange map ..... non-blockable 20 x 20 interchange matrix

E1 link parameters

CRC4 multi-frame synchronism ..... Yes (enabled), No (disabled)
Response to loss of synchronization ..... The A bit of timeslot 0 (Remote Alarm), “blue code” (AIS)
Receiver path sensitivity ..... -36 dB (-43 dB for 19” rack models), -12 dB
Idle code ..... 0x00 - 0xFF

Digital port parameters

Operating mode ..... Sync (synchronous), Async (asynchronous)
Transmission rate in the asynchronous mode ..... 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200 bit/sec
Asynchronous symbol formal 8N1, 7P1, 8P1
Receiver path synchronization mode ..... RXC, ERC, HDLC Buffer
CTS signal generation mode ..... CTS=1, CTS=CD, CTS=RTS, CTS=CD*RTS
RXC/ERC clocks ..... Normal, Inverted
TXC/ETC clocks ..... Normal, Inverted

Ethernet port parameters

	E1-DXC/B/3E1-ETH	E1-DXC/B/3E1-ETV
Operating mode	10 Mbps Half duplex, 10 Mbps Full duplex	10 Mbps Half duplex, 10 Mbps Full duplex, 100 Mbps Half duplex, 100 Mbps Full duplex, Autonegotiation
Packet filtering	Enabled, Disabled	Enabled, Disabled

underflows. The frequency of these errors depends on the discrepancy value between these two frequencies. In cases when it is not possible to provide common clock, and the data transmitted over the network comply with the HDLC protocol, the HDLC mode of the FIFO buffer must be used.

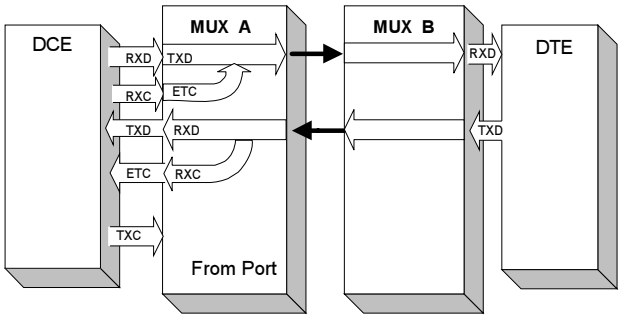
Clock parameter requirements

Clock may be received from the internal generator of the E1-DXC multiplexing cross-connector, or from digital port external clock input. The clock that is used to generate the E1 link output signal, determines such parameters as phase jitter and frequency accuracy. In those modes, when the E1-DXC multiplexing cross-connector is selected as the clock source, the multiplexer technical solutions guarantee, that phase jitter and frequency accuracy comply with the requirements of the corresponding ITU-T recommendations. If another device connected to the E1-DXC digital port (DTE emulation mode) is selected as the clock source, then it is required to make sure that the clock parameters comply with ITU-T requirements.

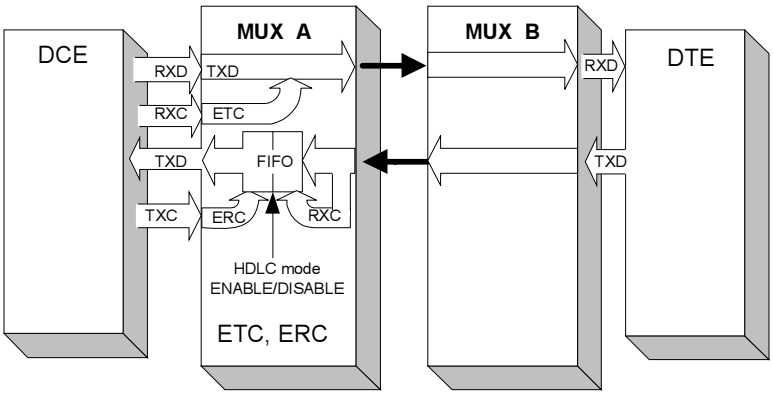
X.21 interface

The X.21 interface has electric signal characteristics complying with the ITU-T V.11 recommendation. The set of signals is different from other interfaces:

X.21 DB-15	Signal
2	Transmit (A)
9	Transmit (B)
4	Receive (A)
11	Receive (B)
7	ETC (A)
14	ETC (B)
6	Sig Timing (A)
13	Sig Timing (B)
3	Control (A)
10	Control (B)
5	Indication (A)
12	Indication (B)
1	Shield
8	GND



DTE1 emulation mode using external transmission clock



DTE2 emulation mode using external transmission and reception clock

Only one clock signal is used in the X.21 interface for received and transmitted data. In order to provide correct data reception, it is required to comply strictly with the requirements for common clock in the link.

The Indication signal corresponds to the CD signal, and the Control signal corresponds to the RTS signal.

Ethernet interface

The E1-DXC/B/3E1-ETH model may be equipped with an Ethernet module with a 10Base-T port, and the E1-DXC/B/3E1-ETV model may be equipped with an Ethernet module with a 10/100BaseT port.

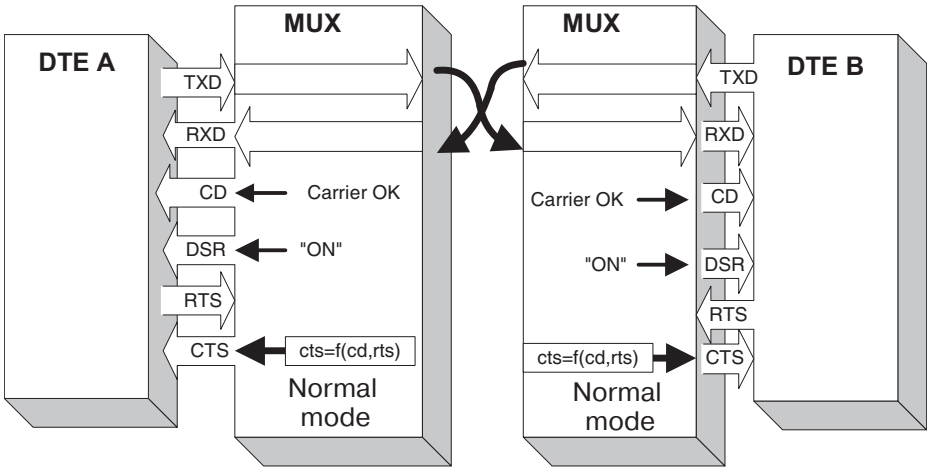
Two devices with Ethernet interface form a remote bridge, and are used for merging two LANs. The remote bridge has the packet filtering capability, that is, it is used to transmit only the packets, the addressees of which are absent from the LAN. Cronyx E1-DXC with an Ethernet interface may perform Ethernet packet compression by clearing packet augmenting bits, the length of which is less than the permitted one.

The remote bridge formed by two devices has the following characteristics:

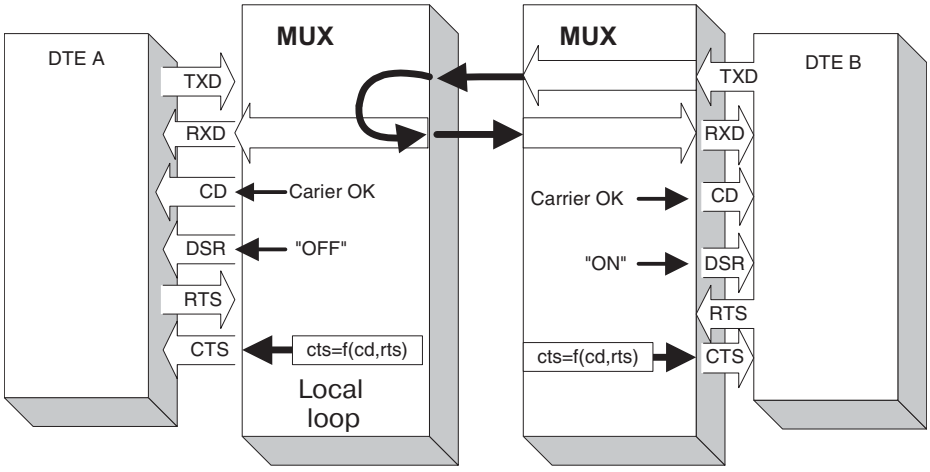
	ETH Module	ETV Module
Connector type	RJ45 (female)	RJ45 (female)
Modes	10 Mbps Half Duplex, 10 Mbps Full Duplex	10 Mbps Half Duplex, 10 Mbps Full Duplex, 100 Mbps Half Duplex, 100 Mbps Full Duplex, Autonegotiation
LAN table	10000 MAC-addresses	15000 MAC-addresses
Max. size of frame	1518 bytes	4228 bytes
Support for VLAN	No	Yes
Protocols	Transparent	Transparent, Cisco-HDLC bridging IEEE protocol

Loops

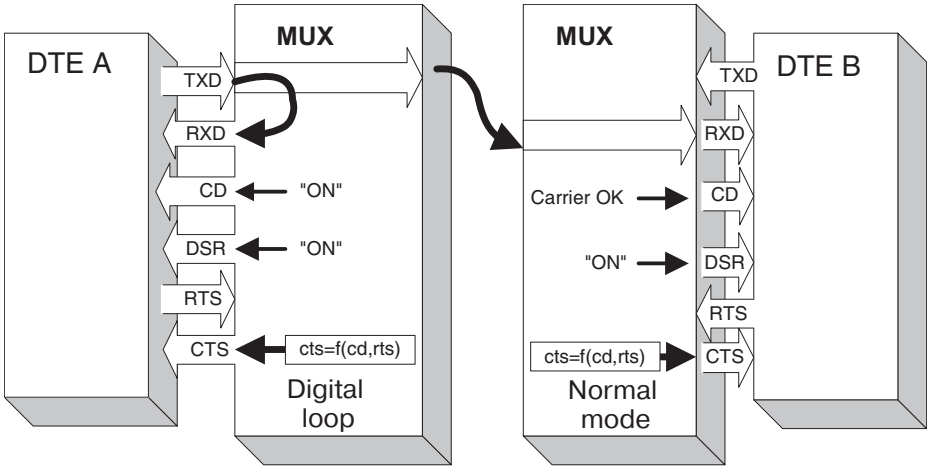
Normal operation



Local loop



Digital loop



Emergency alarms

The emergency alarm interface is used for turning on en external executive unit (ringer, buzzer, console indicator, etc.) during emergency – for example, loss of bearer, loss of synchronization, power failure. It is switched on by "dry" (that is, not connects to any multiplexer electrical circuits) relay contacts.

When power supply and the carrier are present, contact 3 is connected to contact 1. During power or carrier loss, contact 3 breaks circuit 1 and connects to contact 2 (the "alarm" state).

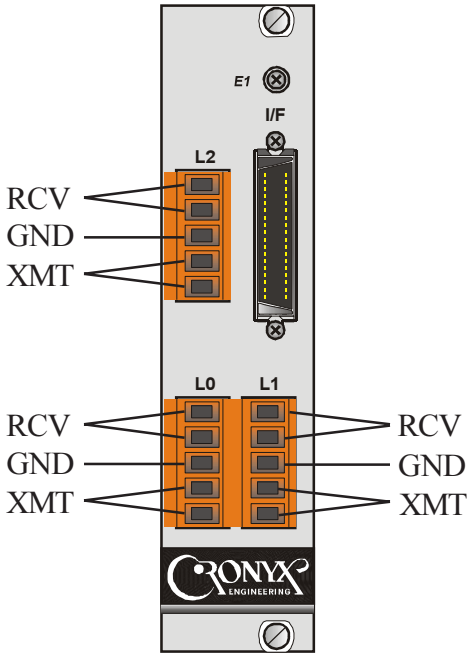
Attention! The 19" design multiplexing cross-connector is not equipped with an emergency alarm interface.

Emergency alarm connector and diagram:

Contact	
1	Connected to the middle contact (3) during normal operation. Disconnected during error
2	Disconnected during normal operations.Connected to the middle contact (3) during error.
3	Middle contact
4	GND
5	Reserved. Must not be connected.
6	GND

Rear panel connectors

The rear panel contains the digital interface connector (for equipped models), and removable E1 link terminals.



Rear panel of the 19" rack device (E1-DXC/R/3E1-M)

In desktop design models digital port with a X.21 interface is equipped with a DB15 connector (female):

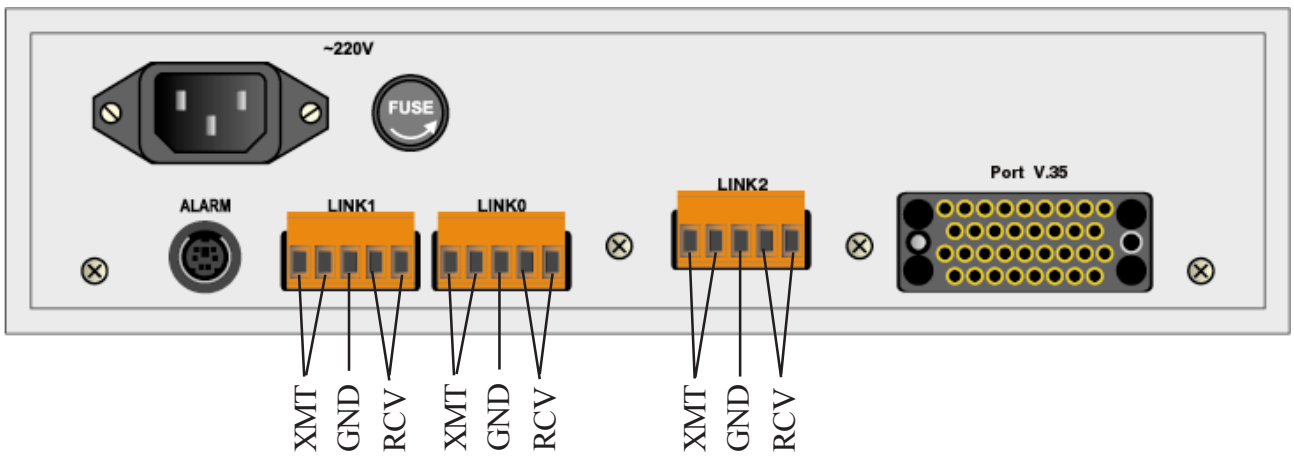
DB-15 female	Signal	Direction
2	T(A)	Receive
9	T(B)	Receive
4	R(A)	Transmit
11	R(B)	Transmit
7	ETC(A)	Receive
14	ETC(B)	Receive
6	S(A)	Transmit
13	S(B)	Transmit
3	C(A)	Receive
10	C(B)	Receive
5	I(A)	Transmit
12	I(B)	Transmit
1, 8	GND	—

In desktop design models the digital port with RS-232 or RS-530 interface is equipped with a DB25 connector (female):

Cont. DB25	RS-530	RS-232	Direction.
2	TXD-a	TXD	Receive
14	TXD-b	—	Receive
3	RXD-a	RXD	Transmit
16	RXD-b	—	Transmit
24	ETC-a	ETC	Receive
11	ETC-b	—	Receive
15	TXC-a	TXC	Transmit
12	TXC-b	—	Transmit
17	RXC-a	RXC	Transmit
9	RXC-b	—	Transmit
21	ERC-a	ERC	Receive
18	ERC-b		Receive
4	RTS-a	RTS	Receive
19	RTS-b	—	Receive
20	DTR-a	DTR	Receive
23	DTR-b	—	Receive
6	DSR-a	DSR	Transmit
22	DSR-b	—	Transmit
5	CTS-a	CTS	Transmit
13	CTS-b	—	Transmit
8	CD-a	CD	Transmit
10	CD-b	—	Transmit
1,7	GND	GND	—

In desktop design models, the digital port with a V.35 interface is equipped with a M-34 connector (female):

Contact	Signal	Direction
P	TD-a	Receive
S	TD-b	Receive
R	RD-a	Transmit
T	RD-b	Transmit
U	ET-a	Receive
W	ET-b	Receive
Y	TC-a	Transmit
AA	TC-b	Transmit
BB	ERC-a	Receive
Z	ERC-b	Receive
V	RC-a	Transmit
X	RC-b	Transmit
C	RTS	Receive
H	DTR	Receive
E	DSR	Transmit
D	CTS	Transmit
F	DCD	Transmit
A	GND	—
B	GND	—



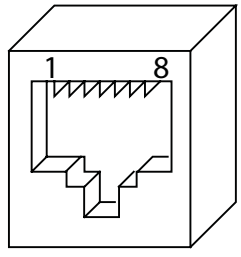
Rear panel of the desktop design device (E1-DXC/B/3E1-V35-AC)

In desktop design models, the digital port with a universal interface is equipped with a HDB44 connector (female):

Cont.	V.35	RS-530	RS-232	X.21
10	TXD-a	TXD-a	TXD	Transmit(A)
25	TXD-b	TXD-b	—	Transmit(B)
8	RXD-a	RXD-a	RXD	Receive(A)
9	RXD-b	RXD-b	—	Receive(B)
6	ETC-a	ETC-a	ETC	ETC(A)
7	ETC-b	ETC-b	—	ETC(B)
2	TXC-a	TXC-a	TXC	SigTiming(A)
3	TXC-b	TXC-b	—	SigTiming(B)
5	RXC-a	RXC-a	RXC	—
4	RXC-b	RXC-b	—	—
17	ERC-a	ERC-a	ERC	—
18	ERC-b	ERC-b	—	—
14	RTS	RTS-a	RTS	Control(A)
29	—	RTS-b	—	Control(B)
11	DTR	DTR-a	DTR	—
26	—	DTR-b	—	—
13	DSR	DSR-a	DSR	—
28	—	DSR-b	—	—
15	CTS	CTS-a	CTS	—
30	—	CTS-b	—	—
12	CD	CD-a	CD	Indication(A)
27	—	CD-b	—	Indication(B)
1,16	GND	GND	GND	GND
31	SEL-0*	SEL-0*	SEL-0*	SEL-0
33	SEL-1	SEL-1*	SEL-1	SEL-1*
35	SEL-2	SEL-2	SEL-2*	SEL-2
37	SEL-3	SEL-3*	SEL-3*	SEL-3*
39	SEL-4*	SEL-4	SEL-4	SEL-4
41	SEL-5*	SEL-5	SEL-5	SEL-5
43	SEL-6*	SEL-6	SEL-6	SEL-6
32	DCE	DCE	DCE	DCE

* - Connect the contact to GND

The Ethernet port is equipped with a RJ-45 connector (female):



1	TD+
2	TD-
3	RD+
4	Not used
5	Not used
6	RD-
7	Not used
8	Not used

In 19" rack mounting design models the digital port with a universal interface is equipped with a MDB36 connector (female):

Cont.	V.35	RS-530	RS-232	X.21
17	TXD-a	TXD-a	TXD	Transmit(A)
18	TXD-b	TXD-b	—	Transmit(B)
12	RXD-a	RXD-a	RXD	Receive(A)
11	RXD-b	RXD-b	—	Receive(B)
19	ETC-a	ETC-a	ETC	ETC(A)
21	ETC-b	ETC-b	—	ETC(B)
32	ERC-a	ERC-a	ERC	SigTiming(A)
34	ERC-b	ERC-b	—	SigTiming(B)
3	TXC-a	TXC-a	TXC	—
4	TXC-b	TXC-b	—	—
13	RXC-a	RXC-a	RXC	—
14	RXC-b	RXC-b	—	—
15	RTS	RTS-a	RTS	Control(A)
16	—	RTS-b	—	Control(B)
1	DTR	DTR-a	DTR	—
2	—	DTR-b	—	—
10	DSR	DSR-a	DSR	—
9	—	DSR-b	—	—
8	CTS	CTS-a	CTS	—
7	—	CTS-b	—	—
6	CD	CD-a	CD	Indication(A)
5	—	CD-b	—	Indication(B)
20,22, 24,26, 28,30		GND	GND	GND
23	SEL-0*	SEL-0*	SEL-0*	SEL-0
25	SEL-1	SEL-1*	SEL-1	SEL-1*
27	SEL-2	SEL-2	SEL-2*	SEL-2
29	SEL-3	SEL-3*	SEL-3*	SEL-3*
31	SEL-4*	SEL-4	SEL-4	SEL-4
33	SEL-5*	SEL-5	SEL-5	SEL-5
35	SEL-6*	SEL-6	SEL-6	SEL-6
36	DCE	DCE	DCE	DCE

* - Connect the contact to GND

Control via the console

The front panel of the multiplexing cross-connector is equipped with a DB9 (female) connector for connecting a control terminal (console) with RS-232 interface . The console may be used for viewing current device modes, link states, error statistics, for selecting device modes, and for storing them in nonvolatile RAM.

The console interface is designed as a simple hierarchical menu. To select a command, you must enter its number.

```
Cronyx E1-DXC /ETH revision B, 27/01/2004

Clocks: Active=Int, Master=Int, Timeslot16=CAS
Link 0: TP, High gain, no CRC4, Idle=0xd5
Link 1: TP, High gain, no CRC4, Idle=0xd5
Link 2: TP, High gain, no CRC4, Idle=0xd5
Port: 1920 kbps, 10Base-T Half Duplex

  1. Statistics
  2. Event counters
  3. Loopback...
  4. Test...
  5. Configure...
  0. Reset

Command:
```

The “Statistics” mode is used for viewing current information, link operating modes and statistic counters.

```
Statistics: Session #4, 0 days, 0:05:19

Clocks: Active=Int, Master=Int, Timeslot16=CAS
Link 0: TP, High gain, no CRC4, Idle=0xd5
Link 1: TP, High gain, no CRC4, Idle=0xd5
Link 2: TP, High gain, no CRC4, Idle=0xd5
Port: 1920 kbps, 10Base-T Half Duplex

                BPV     OOS     Err     Event   Status
Link 0:         0       0       0       0       Ok
Link 1:         0       0       0       0       Ok
Link 2:         0       0       0       0       Ok
Port:           -       -       0       0       Ok

C - clear counters, R - refresh mode, any key to break...
```

The “C” key allows clearing error counters of a local device. The “R” key allows changing the display update mode.

Counter	Error type
BPV	Line encoding violation
OOS	Number of seconds during which frame or multi-frame synchronization was lost
Err	For E1 links - number of seconds during which BER tester errors were present; for serial ports - number of seconds during which external clock errors were present; for Ethernet ports - Ethernet bridge internal buffers overflow.
Event	Number of seconds, during which link-related events have taken place. The meaning of an event depends on the interface type.

Event counter values:

Interface type	Event	Cause
Serial	FIFO buffer error	1. In the DTE2 mode (use of ERC pulses) the requirement of-common clock for the link is not fulfilled. 2. In mode with HDLC buffer disabled too great clock frequency deviation is present, which may mot be compensated by flag insertion/ deletion.
Async	FIFO buffer error	1. Transmission rate or asynchronous symbol format set for the-port, do not correspond to connected-device settings. 2. Too large transmission rate deviation in the connected device from the rated value
IDSL	FIFO buffer error	The requirement for common clock in the link is not fulfilled
E1	Controlled slip (Slip-operation)	The requirement for common clock in the link is not fulfilled
Ethernet	Collision	High Ethernet network segment load

The state of E1 links is shown as a set of flags:

Flag	Link state
OK	Normal mode, frame and multi-frame synchronism present
LOS	Loss of signal in the line
AIS	Reception of alarm indication signal (“blue code”)
LOF	Loss of frame synchronism
LOMF	Loss of multi-frame synchronism
FARLOF	Loss of frame synchronism at the remote device
AIS16	Reception of alarm indication signal in timeslot 16
RDMA	Loss of CAS multi-frame synchronism at the remote modem
CRCE	CRC error
RCRCE	CRC error at the remote modem

The “Loopback” menu is designed for local loop control:

```
Loopback

Clocks: Active=Int, Master=Int, Timeslot16=CAS
Link 0: TP, High gain, no CRC4, Idle=0xd5, Loop
Link 1: TP, High gain, no CRC4, Idle=0xd5
Link 2: TP, High gain, no CRC4, Idle=0xd5
Port: 1920 kbps, 10Base-T Half Duplex

  1. Link 0 loop - enabled
  2. Link 1 loop - disabled
  3. Link 2 loop - disabled

Command:
```

The “Test” menu enables/disabled the built-in BER tester:

```
BER Test

Clocks: Active=Int, Master=Int, Timeslot16=CAS
Link 0: TP, High gain, no CRC4, Idle=0xd5, Test
Link 1: TP, High gain, no CRC4, Idle=0xd5
Link 2: TP, High gain, no CRC4, Idle=0xd5
Port: 1920 kbps, 10Base-T Half Duplex

  1. Link 0 test - run
  2. Link 1 test - stopped
  3. Link 2 test - stopped

Command:
```

Loop and BER tester modes are not stored in the nonvolatile RAM.

The “Configure”’ menu allows selecting device operating modes:

```
Configure

Clocks: Active=Int, Master=Int, Timeslot16=CAS
Link 0: TP, High gain, no CRC4, Idle=0xd5
Link 1: TP, High gain, no CRC4, Idle=0xd5
Link 2: TP, High gain, no CRC4, Idle=0xd5
Port: 1920 kbps, 10Base-T Half Duplex

  1. Sync & cross-connection...
  2. Link 0...
  3. Link 1...
  4. Link 2...
  5. Port...
  7. Factory settings...
  8. Save parameters
  9. Restore parameters

Command:
```

After setting parameters, they must be saved in the multiplexer's nonvolatile RAM (NVRAM) using the "Save parameters" command. The last saved configuration parameters may be restored using the "Restore parameters" command.

The "Sync & cross-connection" menu allows to select master and backup clock, the timeslot 16 mode, and to go to the timeslot and Sa bits interchange map settings menu.

```
Sync & cross-connection

Clocks: Active=Int, Master=Int, Timeslot16=CAS
Link 0: TP, High gain, no CRC4, Idle=0xd5
Link 1: TP, High gain, no CRC4, Idle=0xd5
Link 2: TP, High gain, no CRC4, Idle=0xd5
Port: 1920 kbps, 10Base-T Half Duplex

  1. Master clock: Int
  3. Timeslot interchange map...
  4. Timeslot 16: CAS
  5. E1 link for port data: Link 0
  6. Timeslots for port data...
  7. Sa bits...

Command:
```

The "Timeslot interchange map" allows specifying the interrelationship between the output of single timeslot, and the input of another.

The "d" (data) symbol denotes timeslots used for data transmission. The fixed delay mode will be automatically specified for such timeslots. This mode maintains the integrity of the data stream transmitted over several timeslots.

The "v" (voice) symbol denotes timeslots occupied by voice telephone stream.

```
Timeslots interchange map

TS Link 0   Link 1   Link 2   Port       TS Link 0   Link 1   Link 2   Port
 1 Port     Idle     Idle     d/L0/T1    17 Port     Idle     Idle     d/L0/T17
 2 Port     Idle     Idle     d/L0/T2    18 Port     Idle     Idle     d/L0/T18
 3 Port     Idle     Idle     d/L0/T3    19 Port     Idle     Idle     d/L0/T19
 4 Port     Idle     Idle     d/L0/T4    20 Port     Idle     Idle     d/L0/T20
 5 Port     Idle     Idle     d/L0/T5    21 Port     Idle     Idle     d/L0/T21
 6 Port     Idle     Idle     d/L0/T6    22 Port     Idle     Idle     d/L0/T22
 7 Port     Idle     Idle     d/L0/T7    23 Port     Idle     Idle     d/L0/T23
 8 Port     Idle     Idle     d/L0/T8    24 Port     Idle     Idle     d/L0/T24
 9 Port     Idle     Idle     d/L0/T9    25 Port     Idle     Idle     d/L0/T25
10 Port     Idle     Idle     d/L0/T10   26 Port     Idle     Idle     d/L0/T26
11 Port     Idle     Idle     d/L0/T11   27 Port     Idle     Idle     d/L0/T27
12 Port     Idle     Idle     d/L0/T12   28 Port     Idle     Idle     d/L0/T28
13 Port     Idle     Idle     d/L0/T13   29 Port     Idle     Idle     d/L0/T29
14 Port     Idle     Idle     d/L0/T14   30 Port     Idle     Idle     d/L0/T30
15 Port     Idle     Idle     d/L0/T15   31 Port     Idle     Idle     d/L0/T31

Link 0, Timeslot 1 : Data,  Transmit from Port

 Arrow keys to move, <Enter> to edit, <Ctrl-C> to quit
```

In the 19" rack design, timeslots are always interchanges with a fixed delay, and specifying the "voice" - "data" mode is not required.

The "Sa bits interchange map" menu is used to specify the Sa bits interchange map:

```
Sa bits interchange map

Bit       Link 0          Link 1          Link 2
Sa4     Link 1 Sa7      Set to "1"      Set to "1"
Sa5     Set to "1"      Set to "1"      Set to "1"
Sa6     Set to "1"      Set to "1"      Set to "1"
Sa7     Set to "1"      Link 0 Sa4      Set to "1"
Sa8     Set to "1"      Set to "1"      Set to "1"

Link 0, Sa4: Transmit from Link 1, Sa7


Link 0 Sa bits:

  0. Transmit from Link 0
  1. Transmit from Link 1
  2. Transmit from Link 2
  4. Transmit all "1"


Arrow keys to move, <Enter> to edit, <Ctrl-C> to quit
```

The "Link 0" menu allows setting parameters for the E1/0 link:

```
Link 0

Clocks: Active=Int, Master=Int, Timeslot16=CAS
Link 0: TP, High gain, no CRC4, Idle=0xd5
Link 1: TP, High gain, no CRC4, Idle=0xd5
Link 2: TP, High gain, no CRC4, Idle=0xd5
Port: 1920 kbps, 10Base-T Half Duplex

  4. Crc4: No
  5. Receiver gain: High
  6. Idle code: 0xd5
  7. Loss of sync action: Remote Alarm

Command:
```

To set parameter for other E1 links use menus "Link 1", "Link 2", and "Link 3" which are the same.

In models equipped with a digital port, the “Port” menu is used to set its parameters.

```
Port

Clocks: Active=Int, Master=Int, Timeslot16=CAS
Link 0: TP, High gain, no CRC4, Idle=0xd5
Link 1: TP, High gain, no CRC4, Idle=0xd5
Link 2: TP, High gain, no CRC4, Idle=0xd5
Port: 1920 kbps, 10Base-T Half Duplex

  6. Duplex: Half
  7. Filtering: Enabled

Command:
```

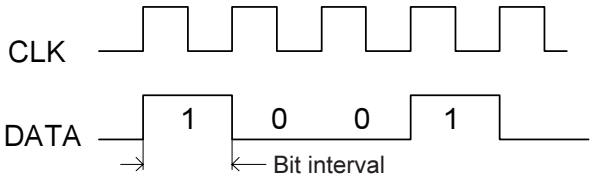
```
Port

Clocks: Active=Int, Master=Int, Timeslot16=CAS
Link 0: TP, High gain, no CRC4, Idle=0xd5
Link 1: TP, High gain, no CRC4, Idle=0xd5
Link 2: TP, High gain, no CRC4, Idle=0xd5
Port: 0 kbps, CTS=1, Cable not attached
        DSR, CTS, no CD, no TXC, no RXC

  4. Mode: Sync
  5. Receive clock: Receive
  6. Transmit data strobe: Normal (data valid on falling edge)
  7. Receive data strobe: Normal (data valid on falling edge)
  8. CTS = 1
  9. HDLC buffer: Disabled

Command:
```

In order to speed up parameters setting it is possible to use one of the three factory presets for the most widespread types of multiplexer usage, with subsequent correction of some parameters:

```
Factory settings

Clocks: Active=Int, Master=Int, Timeslot16=CAS
Link 0: TP, High gain, no CRC4, Idle=0xd5
Link 1: TP, High gain, no CRC4, Idle=0xd5
Link 2: TP, High gain, no CRC4, Idle=0xd5
Port: 1920 kbps, 10Base-T Half Duplex

  1. Empty
  2. Loopback
  3. Link 0 <-> Link 1, Link 2 <-> Port

Command:
```

Synchronous data transfer.

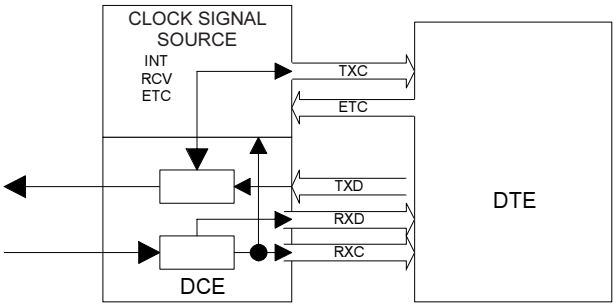
During synchronous data transfer, their modification is performed in strictly determined points of time, which are related to a special clock. The time during which data may not be modified, is called a bit interval. The receiver device must read data during points of time, which are close to the middle of the bit interval. Reading data at a bit interval boundary leads to faults. As a rule, the transmitter device modifies data at one of the clock signal edges, (for example, at the rising edge), and the receiver device reads the data at the other edge (the falling edge in this case).



Different interfaces use different clock signal transmission modes. V.35, RS-530, RS-232 etc., interfaces have special dedicated clock lines for each data direction (receive and transmit). Received RXD data are accompanied by RXC clock, and transmitted TXD data are accompanied by TXC clock.

Line modem interfaces (G.703, xDSL, etc.) use self-synchronizing codes (HDB3, Manchester, 2B1Q, etc.) to transmit data and clock over the same wires. The self-synchronizing codes are characterized by the fact that they do not contain long sequences of the same layer. This allows using the phase lock circuit at the receiver side to extract clock and data from the received signal.

V.35, RS-530, RS-232 interfaces may be of DCE and DTE types. Modems have DCE interfaces, while computer-like devices have DTE. DCE device types are clock sources for both data transmission directions – both signals, the RXC (received data clock) and the TXC (transmitted data clock) are output signals for them. Here the RXC – is a signal received by the modem from the line, and extracted by the phase lock circuit. It accompanies the RXD data received by the modem and has the same direction.



Data received by the modem (TXD), are accompanied by the TXC clock. A DTE device serves as a TXD data signal source. The TXC clock comes from the modem, and its source may be an internal modem clock oscillator (INT), the clock signal extracted by the phase lock circuit from the signal received from the line (RCV), or an external clock source (EXT). As a rule, the external source is the signal received at the ETC interface input.

During serial data transfer, in addition to bit synchronization, there is need to determine byte boundaries. The stream is divided into frames for this purpose. The beginning of the frame serves as the byte reference point. In order to transmit digitized telephone data, the frame format described in the ITU G.704 recommendation is used. The HDLC standard is the most widely spread way to convert bit streams into frames in computer networks.

FLAG	ADDRESS	CONTROL	DATA	CRC	FLAG

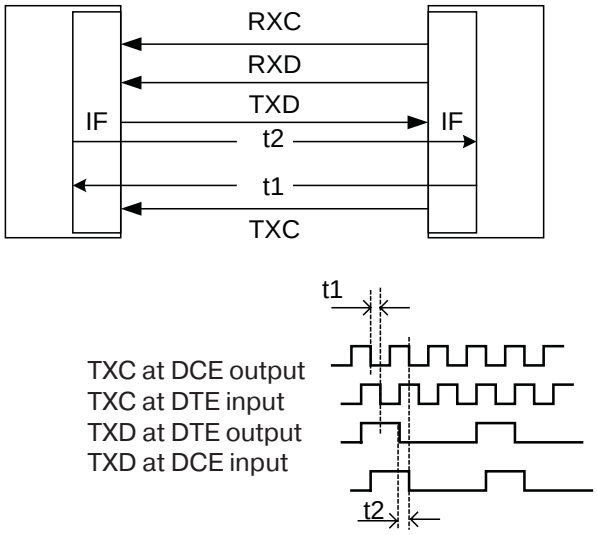
HDLC frame format

A certain bit sequence, called a flag, serves as a frame separator. In the HDLC protocol the flag is 01111110. In this case, in order for this sequence not to appear inside data, the staffing/destaffing procedure is used to insert/remove zeroes in a sequence of ones, which length exceeds five.

Synchronous link design problems.

As a rule, synchronous links are designed on the common clock principle. This means that a data transmission link between two DTE devices uses a single clock to synchronize all data streams in the link. Clock is transmitted on the DCE-DTE device junction over special lines, and with the

help of self-synchronizing codes over communication lines. In a simplest case, when connecting two routers equipped with V.35 interfaces using synchronous modems for a dedicated line, the clock source is the internal oscillator of one of the modems (INT). The second modem extracts the clock from the signal received from the line (RCV). Both routers, as DTE devices, receive clock from modems.

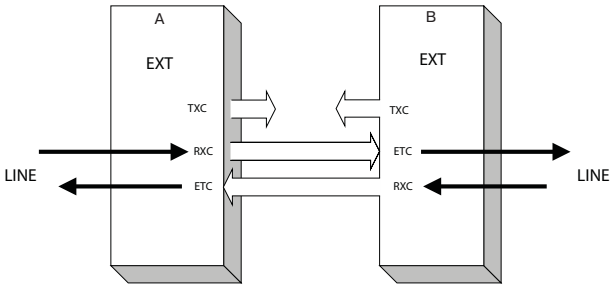


Data are modified at the rising edge, and strobe at the falling edge.
An error situation is shown. Due to strobbing data input the DCE device during their modification

The problem that may arise even in this simplest case, is caused by the fact that the data received by the modem (TXD), and the clock accompanying them (TXC) have different directions, and are transmitted with delays. The TXC signal arrives to the DTE with a delay of t1, which is determined by internal modem circuits, connecting cables and the router interface. At the rising edge of the TXC signal, the router modifies the TXD data, which, after passing in the reverse direction, arrive to the modem with a delay of t2. If the sum of these two delays t1 + t2 is equal to the clock half-period, then data modification at the input comes precisely to the edge, which is used by the modem to sample data.

This leads to erroneous data reception from the router. The probability of such a situation increases as data transmission rate rises. This situation may be amended by inverting the TXC clock signal. This may be performed by changing the corresponding setting in the configuration of one of the devices.

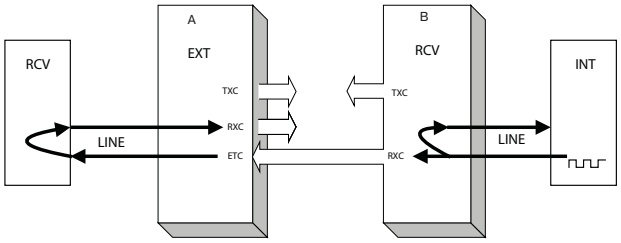
In some cases, there is a need to connect two DCE devices over V.35, RS-232, RS-530, etc. interface. The simplest way to make such a connection is to use the external clock mode for the transmitter path (EXT) for both devices.



Connection of two DCE devices over a digital interface.
The clock transmission path is shown.

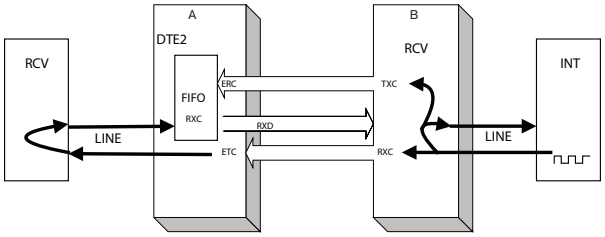
In this mode, the modem transmits data to the line according to the clock signal received at the ETC interface input. The data received from the line by the first modem, and the accompanying clock signal arrives to RXD and RXC outputs. A special cable is used to supply them to, respectively, TXD and ETC inputs of the second modem, which transmits data and clock further to the line. The reverse stream passes over the same path. In this case the data and clock received from the line are relayed. This means that the clock source is external to the devices in question.

It is possible when the single device does not support the transmitter path synchronization from the external source (EXT). In this case, it is only possible to set the transmitter path synchronization from the ETC input for one of the modems. Here the modem that does not support this mode, will receive data at the TXD input using the clock from its internal clock source (INT) or received from the line (RCV).



Connection of two DCE devices over a digital interface.
Device B does not have a ETC input. The clock transmission path is shown.

If all devices used in the link, are configured to provide common clock, then the clock at the RXC output will have the same frequency (from the same source), as the clock in the transmitter path of the second modem. The link will operate without errors, if the phase shift between those two clocks is not equal to exactly half the period, the probability of which is quite low. In order to eliminate a situation completely, Cronyx synchronous modems support the DTE2 emulation mode. In this mode, the FIFO buffer is enabled on the digital interface in the received data path.



Connection of two DCE devices over a digital interface.
Device A uses a FIFO buffer. The clock transmission path is shown.

Data are put into the buffer according to the clock received from the line, and extracted according to the clock supplied to the ERC pins of the interface connector (external receiving clock). In this way, the FIFO buffer performs clock phase leveling. Here the Cronyx modem emulates a DTE interface, receiving transmission clock at the ETC input, and reception clock at the ERC input. The requirement for common clock is maintained. If there is no way to provide common clock in the link then the clock at one side of the buffer will have a different frequency compared to the clock at the other side of the buffer. This will lead to periodic buffer overflows or underflows, depending on which buffer side the clock has a higher frequency.

If data transmitted over a link are HDLC format packets, then this frequency discrepancy may be compensated using the fact that data in the HDLC stream have gaps filled with a special 01111110 bit sequence – the flag.

In Cronyx modems FIFO buffers may be switched to the HDLC mode. Here the control logic inserts HDLC flags between frames when the buffer tends to underflow, and removes excess HDLC flags when the buffer tends to overflow. The frequency discrepancy, which may be compensated in such a way, depends on HDLC packet length and the amount of flags between packets (this mode may not function when the number of flags between packets is less than two). For IP networks, the typical HDLC frame length is 1500 bytes, and the minimum number of flags between frames is 2. In this case the maximum frequency discrepancy, which may be compensated by such a buffer is at least 200 ppm.

Cable wiring diagrams

V.35 cable for model E1-DXC/B/3E1-M

Signal	HDB44 (male)		M34 (female)
TXD-a	10	←	P
TXD-b	25	←	S
RXD-a	8	→	R
RXD-b	9	→	T
ETC-a	6	←	U
ETC-b	7	←	W
TXC-a	2	→	Y
TXC-b	3	→	AA
RXC-a	5	→	V
RXC-b	4	→	X
ERC-a	17	←	BB
ERC-b	18	←	Z
RTS	14	←	C
DTR	11	←	H
DSR	13	→	E
CTS	15	→	D
CD	12	→	F
GND	1	↔	A
GND	16	↔	B
SEL-x	31,39,41,43 connect to GND 1		

RS-232 cable for model E1-DXC/B/3E1-M

Signal	HDB44 (male)		DB25 (female)
TXD	10	←	2
RXD	8	→	3
ETC	6	←	24
TXC	2	→	15
RXC	5	→	17
ERC	17	←	21
RTS	14	←	4
DTR	11	←	20
DSR	13	→	6
CTS	15	→	5
CD	12	→	8
GND	1	↔	1
GND	16	↔	7
SEL-x	31,35,37 connect to GND 1		

RS-530 cable for model E1-DXC/B/3E1-M

Signal	HDB44 (male)		DB25 (female)
TXD-a	10	←	2
TXD-b	25	←	14
RXD-a	8	→	3
RXD-b	9	→	16
ETC-a	6	←	24
ETC-b	7	←	11
TXC-a	2	→	15
TXC-b	3	→	12
RXC-a	5	→	17
RXC-b	4	→	9
ERC-a	17	←	21
ERC-b	18	←	18
RTS-a	14	←	4
RTS-b	29	←	19
DTR-a	11	←	20
DTR-b	26	←	23
DSR-a	13	→	6
DSR-b	28	→	22
CTS-a	15	→	5
CTS-b	30	→	13
CD-a	12	→	8
CD-b	27	→	10
GND	1	↔	1
GND	16	↔	7
SEL-x	31,33,37 connect to GND 1		

X.21 cable for model E1-DXC/B/3E1-M

Signal	HDB44 (male)		DB15 (female)
TXD-a	10	←	2
TXD-b	25	←	9
RXD-a	8	→	4
RXD-b	9	→	11
ETC-a	6	←	7
ETC-b	7	←	14
TXC-a	2	→	6
TXC-b	3	→	13
RTS-a	14	←	3
RTS-b	29	←	10
CD-a	12	→	5
CD-b	27	→	12
GND	1	↔	1
GND	16	↔	8
SEL-x	33,37 connect to GND 1		

RS-449 cable for model E1-DXC/B/3E1-M

Signal	HDB44 (male)		DB37 (female)
TXD-a	10	←	4
TXD-b	25	←	22
RXD-a	8	→	6
RXD-b	9	→	24
ETC-a	6	←	17
ETC-b	7	←	35
TXC-a	2	→	5
TXC-b	3	→	23
RXC-a	5	→	8
RXC-b	4	→	26
ERC-a	17	←	3
ERC-b	18	←	21
RTS-a	14	←	7
RTS-b	29	←	25
DTR-a	11	←	12
DTR-b	26	←	30
DSR-a	13	→	11
DSR-b	28	→	29
CTS-a	15	→	9
CTS-b	30	→	27
CD-a	12	→	13
CD-b	27	→	31
GND	1	↔	1
GND	16	↔	19
SEL-x	31,33,37 connect to GND 1		

V.35 cable for connecting to DCE, for model E1-DXC/B/3E1-M

Signal	HDB44 (male)		M34 (female)	
TXD-a	10	←	R	RXD-a
TXD-b	25	←	T	RXD-b
RXD-a	8	→	P	TXD-a
RXD-b	9	→	S	TXD-b
ETC-a	6	←	V	RXC-a
ETC-b	7	←	X	RXC-b
RXC-a	5	→	U	ETC-a
RXC-b	4	→	W	ETC-b
RTS	14	←	F	CD
DTR	11	←	E	DSR
DSR	13	→	H	DTR
CD	12	→	C	RTS
TXC-a	2	→	BB	ERC-a
TXC-b	3	→	Z	ERC-b
ERC-a	17	←	Y	TXC-a
ERC-b	18	←	AA	TXC-b
GND	1	↔	A	GND
GND	16	↔	B	GND
SEL-x	31,39,41,43,32 connect to GND 1			

V.35 cable for connecting to the Cronyx Tau-PCI board, for model E1-DXC/B/3E1-M

Signal	HDB44 (male)		HDB26 (male)	Signal
TXD-a	10	←	1	TXD-a
TXD-b	25	←	2	TXD-b
RXD-a	8	→	3	RXD-a
RXD-b	9	→	24	RXD-b
ETC-a	6	←	7	TXCOUT-a
ETC-b	7	←	9	TXCOUT-b
RXC-a	5	→	5	RXCIN-a
RXC-b	4	→	15	RXCIN-b
RTS	14	←	10	RTS
DTR	11	←	19	DTR
DSR	13	→	25	DSR
CD	12	→	16	CD
TXC-a	2	→	22	TXCIN-a
TXC-b	3	→	23	TXCIN-b
ERC-a	17	Not connected		
ERC-b	18	Not connected		
GND	1	↔	11	GND
GND	16	↔	4,6,18	GND
SEL-x	31,39,41,43 connect to GND 1			

V.35 cable for model E1-DXC/R/3E1-M

Signal	MDB36 (female)		M34 (female)
TXD-a	17	←	P
TXD-b	18	←	S
RXD-a	12	→	R
RXD-b	11	→	T
ETC-a	19	←	U
ETC-b	21	←	W
TXC-a	3	→	Y
TXC-b	4	→	AA
RXC-a	13	→	V
RXC-b	14	→	X
ERC-a	32	←	BB
ERC-b	34	←	Z
RTS	15	←	C
DTR	1	←	H
DSR	10	→	E
CTS	8	→	D
CD	6	→	F
GND	20,22,24,26	↔	A
GND	28,30	↔	B
SEL-x	23,31,33,35 connect to GND 28		

RS-232 cable for model E1-DXC/R/3E1-M

Signal	MDB36 (female)		DB25 (female)
TXD	17	←	2
RXD	12	→	3
ETC	19	←	24
TXC	3	→	15
RXC	13	→	17
ERC	32	←	21
RTS	15	←	4
DTR	1	←	20
DSR	10	→	6
CTS	8	→	5
CD	6	→	8
GND	20,22,24,26	↔	1
GND	28,30	↔	7
SEL-x	23,27,29 connect to GND 28		

RS-530 cable for model E1-DXC/R/3E1-M

Signal	MDB36 (female)		DB25 (female)
TXD-a	17	←	2
TXD-b	18	←	14
RXD-a	12	→	3
RXD-b	11	→	16
ETC-a	19	←	24
ETC-b	21	←	11
TXC-a	3	→	15
TXC-b	4	→	12
RXC-a	13	→	17
RXC-b	14	→	9
ERC-a	32	←	21
ERC-b	34	←	18
RTS-a	15	←	4
RTS-b	16	←	19
DTR-a	1	←	20
DTR-b	2	←	23
DSR-a	10	→	6
DSR-b	9	→	22
CTS-a	8	→	5
CTS-b	7	→	13
CD-a	6	→	8
CD-b	5	→	10
GND	20,22,24,26	↔	1
GND	28,30	↔	7
SEL-x	23,25,29 connect to GND 28		

X.21 cable for model E1-DXC/R/3E1-M

Signal	MDB36 (female)		DB15 (female)
TXD-a	17	←	2
TXD-b	18	←	9
RXD-a	12	→	4
RXD-b	11	→	11
ETC-a	19	←	7
ETC-b	21	←	14
TXC-a	3	→	6
TXC-b	4	→	13
RTS-a	15	←	3
RTS-b	16	←	10
CD-a	6	→	5
CD-b	5	→	12
GND	20,22,24,26	↔	1
GND	28,30	↔	8
SEL-x	25,29 connect to GND 28		

RS-449 cable for model E1-DXC/R/3E1-M

Signal	MDB36 (female)		DB37 (female)
TXD-a	17	←	4
TXD-b	18	←	22
RXD-a	12	→	6
RXD-b	11	→	24
ETC-a	19	←	17
ETC-b	21	←	35
TXC-a	3	→	5
TXC-b	4	→	23
RXC-a	13	→	8
RXC-b	14	→	26
ERC-a	32	←	3
ERC-b	34	←	21
RTS-a	15	←	7
RTS-b	16	←	25
DTR-a	1	←	12
DTR-b	2	←	30
DSR-a	10	→	11
DSR-b	9	→	29
CTS-a	8	→	9
CTS-b	7	→	27
CD-a	6	→	13
CD-b	5	→	31
GND	20,22,24,26	↔	1
GND	28,30	↔	19
SEL-x	23,25,29 connect to GND 28		

V.35 cable for connecting to DCE, for model E1-DXC/R/3E1-M

Signal	MDB36 (female)		M34 (female)	
TXD-a	17	←	R	RXD-a
TXD-b	18	←	T	RXD-b
RXD-a	12	→	P	TXD-a
RXD-b	11	→	S	TXD-b
ETC-a	19	←	V	RXC-a
ETC-b	21	←	X	RXC-b
RXC-a	13	→	U	ETC-a
RXC-b	14	→	W	ETC-b
RTS	15	←	F	CD
DTR	1	←	E	DSR
DSR	10	→	H	DTR
CD	6	→	C	RTS
TXC-a	3	→	BB	ERC-a
TXC-b	4	→	Z	ERC-b
ERC-a	32	←	Y	TXC-a
ERC-b	34	←	AA	TXC-b
GND	20,22,24,26	↔	A	GND
GND	28,30	↔	B	GND
SEL-x	23,21,33,35,36 connect to GND 28			

V.35 cable for connecting to the Cronyx Tau-PCI board, for model E1-DXC/R/3E1-M

Signal	MDB36 (female)		HDB26 (male)	Signal
TXD-a	17	←	1	TXD-a
TXD-b	18	←	2	TXD-b
RXD-a	12	→	3	RXD-a
RXD-b	11	→	24	RXD-b
ETC-a	19	←	7	TXCOUT-a
ETC-b	21	←	9	TXCOUT-b
RXC-a	13	→	5	RXCIN-a
RXC-b	14	→	15	RXCIN-b
RTS	15	←	10	RTS
DTR	1	←	19	DTR
DSR	10	→	25	DSR
CD	6	→	16	CD
TXC-a	3	→	22	TXCIN-a
TXC-b	4	→	23	TXCIN-b
ERC-a	32	Not connected		
ERC-b	34	Not connected		
GND	20,22, 24,26	↔	11	GND
GND	28,30	↔	4,6,18	GND
SEL-x	23,31,33,35 connect to GND 28			

V.35 cable for connecting to DCE, for model E1-DXC/B/3E1-V

M34 (male)			M34 (male)	
TXD-a	P	←	R	RXD-a
TXD-b	S	←	T	RXD-b
RXD-a	R	→	P	TXD-a
RXD-b	T	→	S	TXD-b
ETC-a	U	←	V	RXC-a
ETC-b	W	←	X	RXC-b
RXC-a	V	→	U	ETC-a
RXC-b	X	→	W	ETC-b
TXC-a	Y	→	BB	ERC-a
TXC-b	AA	→	Z	ERC-b
ERC-a	BB	←	Y	TXC-a
ERC-b	Z	←	AA	TXC-b
RTS	C	←	F	CD
DTR	H	←	E	DSR
DSR	E	→	H	DTR
CD	F	→	C	RTS
GND	A	↔	A	GND
GND	B	↔	B	GND